What is claimed is:

1. A silicon capacitor formed on an integrated circuit substrate, comprising:

a metal portion on the substrate;

a silicon nitride (SiN) portion sputtered on the substrate; and

a silicon (Si) portion sputtered on the silicon nitride portion.

2. The silicon capacitor of claim 1, wherein the silicon nitride decreases leakage.

3. The silicon capacitor of claim 1, further comprising a second silicon nitride portion.

4. The silicon capacitor of claim 1, further comprising a second metal portion.

5. The silicon capacitor of claim 1, wherein the capacitor is formed using a process including:

depositing metal on the substrate;

sputtering silicon with nitrogen gas to form SiN;

removing nitrogen gas flow to deposit pure silicon;

adding nitrogen gas again to cap the layer with SiN; and

depositing metal.

6. The silicon capacitor of claim 5, wherein each layer deposited is approximately forty angstroms thick.

7. A method for forming a silicon capacitor, comprising:

depositing a metal portion on a substrate;

sputtering a silicon nitride (SiN) portion on the metal portion and the substrate; and

sputtering a silicon (Si) portion.

8. The method of claim 7, further comprising forming a sandwich with layers of SiN and Si.

9. The method of claim 8, further comprising developing a metal layer adjacent to the sandwich.

10. The method of claim 7, wherein the silicon nitride decreases leakage.

11. The method of claim 7, further comprising depositing a second silicon nitride portion.

12. The method of claim 7, further comprising depositing a second metal portion.

13. The method of claim 7, further comprising:

depositing metal on the substrate;

sputtering silicon with nitrogen gas to form SiN;

removing nitrogen gas flow to deposit pure silicon;

adding nitrogen gas again to cap the layer with SiN; and

depositing metal.

14. The method of claim 7, wherein each layer deposited is approximately forty angstroms thick.